

Performance Comparison of CMOS and Finfet Based Circuits At 45nm Technology Using SPICE

Mugdha Sathe*, Dr. Nisha Sarwade**

*(Department of Electrical Engineering, VJTI, Mumbai-19)

** (Department of Electrical Engineering, VJTI, Mumbai-19)

ABSTRACT

According to the Moore's Law, the number of transistors in a unit chip area double every two years. But the existing technology of integrated circuit formation is posing limitations to this law. CMOS technology shows certain limitations as the device is reduced more and more in the nanometer regime out of which power dissipation is an important issue. FinFET is evolving to be a promising technology in this regard. This paper aims to analyze and compare the characteristics of CMOS and FinFET circuits at 45nm technology. Inverter circuit is implemented in order to study the basic characteristics such as voltage transfer characteristics, leakage current and power dissipation. Further the efficiency of FinFET to reduce power as compared to CMOS is proved using SRAM circuit. The results show that the average power is reduced by 92.93% in read operation and by 97.8% in write operation.

Keywords – 6T SRAM cell, CMOS vs FinFET, FinFETs, Low power nanoscale design, Power dissipation

I. Introduction

The integrated circuit technology is progressing at a great pace since the invention of first MOS microprocessor in 1970. The major driving force behind this progress is the technique of scaling. The scaling of MOS transistor has resulted in high density, high performance chips. But this miniaturization is obstructed by many unwanted issues that arise in MOS device as the device size goes on shrinking [1]. Out of these issues, power dissipation is a major drawback. It has been listed as one of the challenges in International Technology Roadmap for Semiconductors (ITRS) 2012. Different low power design techniques using CMOS are implemented but they see certain limitations. Hence the need for new transistor technology arises. In this report, one such technology, FinFET technology is studied. From the perspective of circuit operation, a FinFET behave very much similar to MOSFET. However, two gates provide a greater control over the channel because of which many performance parameters can be altered.

The second section describes in brief about the limitations of CMOS scaling along with how these limitations can be overcome using FinFETs. The third section describes the operation of conventional 6T SRAM cell. In the fourth section the modelling parameters of FinFET and CMOS at 45nm are discussed. The simulation results are presented in the fifth section along with their analysis.

II. Issues in Scaling: CMOS vs FinFET

Short channel effects (SCEs) and leakage current are a major source of power dissipation in MOSFETs

at nanoscale. An effect called drain-induced barrier lowering (DIBL) takes place when a high-drain voltage is applied to a short-channel device and the source injects carriers into the channel surface independent of gate voltage. Gate oxide tunneling of electrons can result in leakage when there is a high electric field across a thin gate oxide layer. Hot-carrier injection occurs in short-channel transistors. Because of a strong electric field near the silicon/silicon oxide interface, electrons or holes can gain enough energy to cross the interface and enter the oxide layer. Punchthrough leakage occurs when there is decreased separation between depletion regions at the drain-substrate and the source-substrate junctions.

The front and back gates are electrically coupled to better control Short Channel Effects by substantially lowering both Drain Induced Barrier Lowering and sub-threshold slope (S). Therefore, FinFET devices are most suitable for low-power designs as they enable significant reduction in standby power while simultaneously providing increased performance [2]. Joshi, Kim and Kanj have analyzed in [2] the DG-nFET device. They have proved that a DG-MOSFET shows far superior device characteristics to its bulk-Si counterparts with much lower sub-threshold slope S (65 mV/V vs. 90 mV/V) and much suppressed DIBL (35 mV/V vs. 105 mV/V), which offer over 10 times reduced off-current.

In order to overcome the issues regarding power dissipation, certain low power design techniques using CMOS are implemented [3]. Reduction in power dissipation can be achieved by reducing the

supply voltage but this has a disadvantage of increasing the delay. Reduction in threshold voltage increases leakage current. Lowering the capacitance have adverse effects on the system performance.

The low power techniques employed for FinFET circuits effectively reduce the power of the circuit at the same time overcoming the above issues of CMOS techniques. The advantages of these techniques are summarized in [4]. Back-Gate biasing technique reduces V_T variability, reduces leakage and thus power [1]. Dual- V_T technique enables merging of transistors thus saving up on total power [5]. Asymmetric- Φ_G produces low leakage current and high speed performance [6].

III. Operation of Conventional 6T SRAM Cell

The conventional 6T SRAM cell using FinFETs is shown in Figure 1. This cell is made up six transistors. Two pairs of inverters are connected such that the output of one is fed to the input of the other and vice versa. This feedback connection stabilizes the storage nodes in the cell. Two other transistors are used as access transistors and are connected to the storage nodes (Q and QB) of the two inverters. The signals wordline (WL), bitline (BL) and bitlinebar (BLB) control the operation of the cell. When WL is high, the access transistors are turned on providing the access to the storage nodes. For write operation, BL and BLB are set according to the value to be written (complement of each other) and Q and QB are pulled to the required levels. For read operation, BL and BLB are precharged to high voltage. Either BL or BLB discharge depending upon the values of Q and QB, thus data is read.

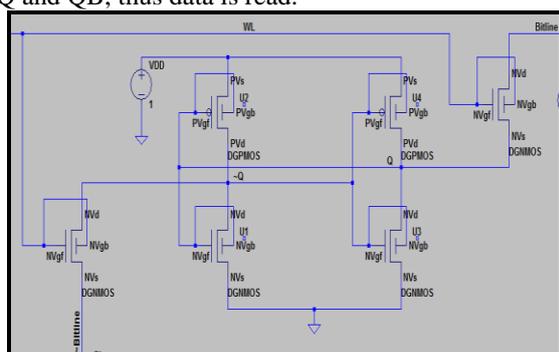


Fig. 1. 6T SRAM cell using FinFET

IV. Modelling Parameters of FinFET at 45nm

The key parameters of the FinFET model are its gate length (L_g), height of the fin (H_{fin}), thickness of gate oxide (t_{ox}), thickness of the fin (T_{si}) and the channel width. These parameters define the performance of the circuit. They are important to minimize leakage current at the same time maintaining the on current. The model files used in here are PTM model files [7]. The values of the

parameters used in this model of FinFET at 45nm are given in TABLE 1.

Table 1. Modelling parameters of FinFET at 45nm

Parameter	Value
Channel length (L_g)	45nm
Oxide Thickness (t_{ox})	1.5nm
Si thickness (T_{si})	8.4nm
Threshold voltage of front gate (V_{thf0})	0.31V
Threshold voltage of back gate (V_{thb0})	0.31V
Channel doping (N_{ch})	$2*10^{16} \text{ cm}^{-3}$

V. Simulation Results

In order to prove the claim that FinFETs give better performance in terms of power dissipation and leakage current than CMOS, simple inverter circuit is used. Inverter circuits using FinFETs and using CMOS at 45 nm are formed. They are simulated by varying the input voltage from 0 to 1V at intervals of 0.001V.

In Figure 2, the voltage transfer characteristics (VTC) of FinFET inverter and CMOS inverter at 45 nm are compared. From the figure it is evident that the VTC curve for CMOS is steeper than that of FinFET. This is an advantage of CMOS over FinFET.

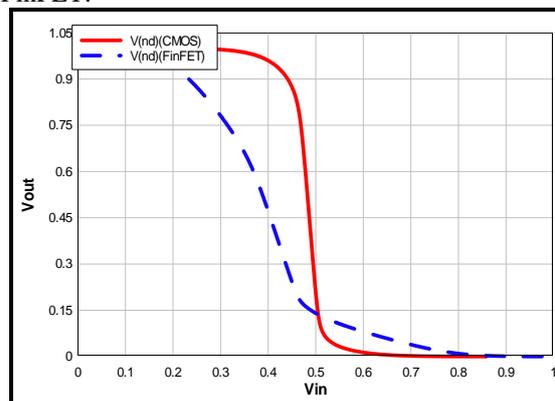


Fig. 2. Voltage transfer characteristics of FinFET and CMOS at 45 nm node

In Figure 3, the power dissipation in the NMOS device of FinFET and CMOS inverters is compared. It can be seen that the peak power dissipated in CMOS circuit is 120uW whereas in FinFET circuit it is 22uW. The average power dissipation over the given range of input voltage is found to be 12.8uW in CMOS inverter and 5.2uW in FinFET inverter resulting in a 59.38% reduction.

Also the gate leakage current was observed to reduce from 1.8nA in CMOS to 0.0012fA in FinFET.

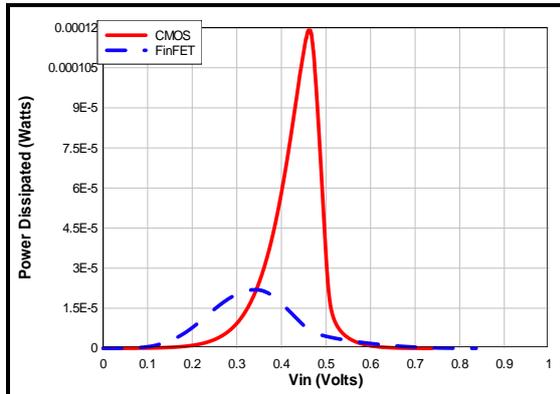


Fig. 3. Power dissipation of NMOS in FinFET and CMOS inverters at 45 nm node

Figures 4 and 5 show the write operations of SRAMs implemented using CMOS and FinFET respectively. The simulation is performed for a period of 75us. The bit line (BL) is first made high. Then after some time, the word line (WL) is made high. It can be seen that at that particular instant (35us), the storage bit (Q) becomes high. Thus write operation is achieved.

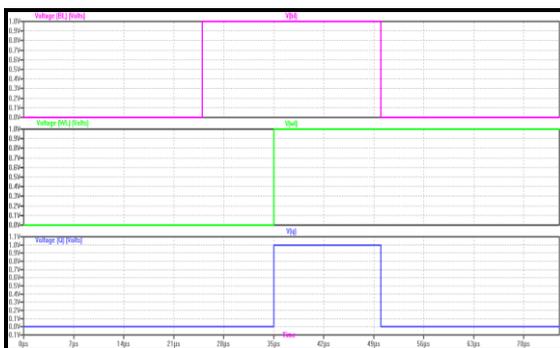


Fig. 4. Write operation of CMOS SRAM

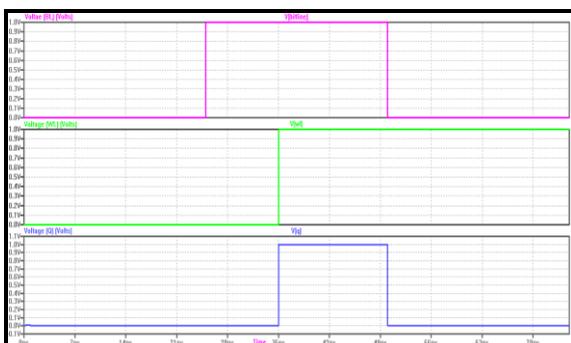


Fig. 5. Write operation of FinFET SRAM

In the successive two figures (6 and 7), the power dissipation of these two SRAM circuits during write operation is shown. It shows the total switching power of all the four transistors forming the two inverters since switching takes place at these

transistors. In both the figures, the first plot is of V(Q) i.e. voltage at storage node Q. The instant at which Q becomes 1 is the write 1 instant (35us) and the instant at which Q become 0 is the write 0 instant (50us). It can be seen that power dissipation in all the transistors occur at these two instances. Adding up the power of the four transistor, the total switching power dissipation of CMOS at write 1 is 587.9uW and that of FinFET is 9.76uW.

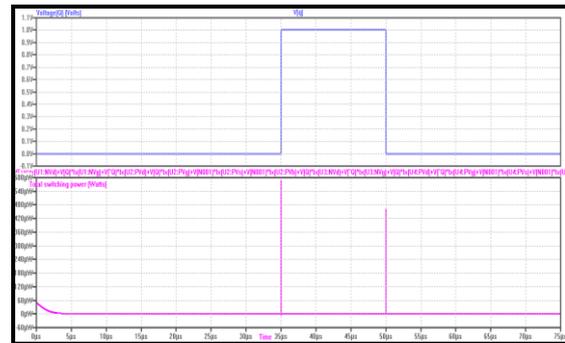


Fig. 6. Total switching power in CMOS SRAM during write operation

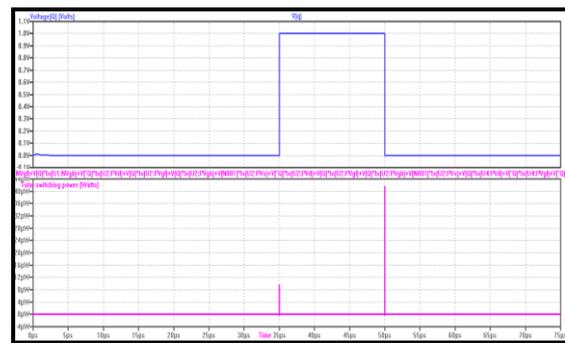


Fig. 7. Total switching power in FinFET SRAM during write operation

Figures 8 and 9 show read operations of CMOS and FinFET SRAMs respectively. It can be seen that equivalent performance is obtained using FinFET instead of CMOS in the write and read operation.

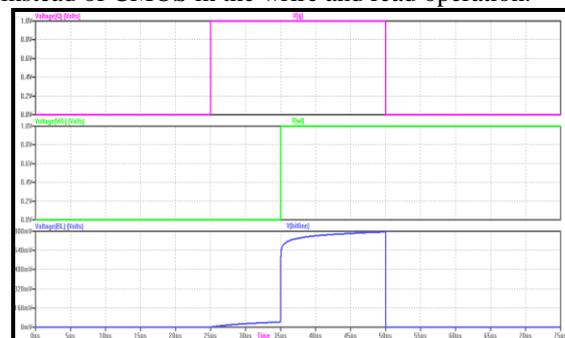


Fig. 8. Read operation of CMOS SRAM

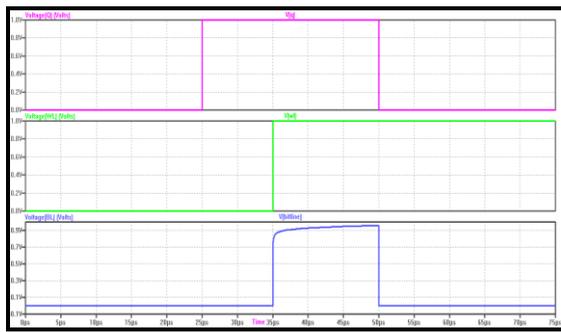


Fig. 9. Read operation of FinFET SRAM

Figures 10 and 11 show the power dissipation of CMOS SRAM and FinFET SRAM respectively during read operation.

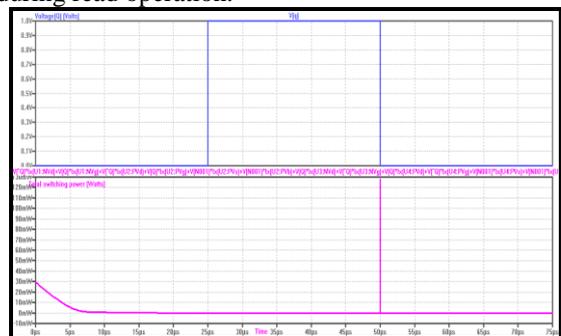


Fig. 10. Total switching power in CMOS SRAM during read operation

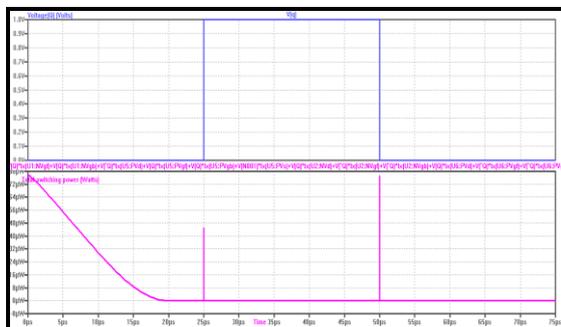


Fig. 11. Total switching power in FinFET SRAM during read operation

VI. Conclusion

The limitations of CMOS scaling are reviewed. It is observed that FinFETs are capable to overcome these limitations effectively. The comparison of inverter circuits using CMOS and FinFETs at 45nm show that power reduction by 59.38% is achieved in FinFET circuit. Although it faces the disadvantage of a slower voltage transfer characteristics as compared to CMOS.

The simulations of read and write operations of SRAM cell are found to be same using FinFETs and CMOS. Whereas the results of the switching power show a large reduction in the power using FinFETs than using CMOS. The results are tabulated below in TABLE 2.

Table 2. Comparison of obtained results

Performance Parameter	CMOS	FinFET	% change in FinFET as compared to CMOS
Average Power in SRAM Read Operation	124uW	8.76uW	92.93% reduction
Average Power in SRAM Write Operation	896.17nW	19.76nW	97.8% reduction
Average Power in 45nm Inverter	12.8uW	5.2uW	59.38% reduction

The results obtained from the simulation of SRAM cell help to prove that FinFETs can be used to reduce power without compromising on the performance.

References

- [1] B. Swahn and S. Hassoun, "Gate Sizing: FinFETs vs 32nm Bulk MOSFETs", *Design Automation Conference, 2006 43rd ACM/IEEE*, San Francisco, CA, 2006, 528-531.
- [2] R. Joshi, K. Kim and R. Kanj, "FinFET SRAM Design", in *Nanoelectronic Circuit Design, Springer*, 2011, 55-95.
- [3] Jan M. Rabaey *Digital Integrated Circuits: A Design Perspective* (Prentice-Hall of India Pvt. Ltd, New Delhi, October 2001).
- [4] M. Sathe and N. Sarwade, "Power Optimization at Nanoscale using FinFETs and its Comparison with CMOS", *International Journal of Computer Engineering and Applications*, vol. 6, issue II, May 14, 33-41.
- [5] M. Rostami and K. Mohanram, "Dual-Vth Independent-Gate FinFETs for Low Power Logic Circuits", *IEEE Transactions on Computer-Aided Design Of Integrated Circuits And Systems*, vol. 30, no. 3, March 2011, 337-349.
- [6] N. Bhoj and N. K. Jha, "Design of Ultra-low-leakage Logic Gates and Flip-flops in High-performance FinFET Technology", *International Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, March 2011, 1-8.
- [7] Predictive Technology Modelling URL: <http://ptm.asu.edu/>

About the Authors

Mugdha S. Sathe received the B.E. degree in Electronics Engineering from Mumbai University, India, in 2011. She is currently pursuing the M.Tech. degree in Electronics Engineering under guidance of Dr. Nisha Sarwade at Veermata Jijabai Technological Institute, Mumbai, India.

Dr. Nisha P. Sarwade received the B.E. degree in Electronics Engineering from Jiwaji University, Gwalior and M.E. (Solid State Electronics) and PhD (Electronics Engineering) from University of Roorkee. She was working as a lecturer at the University of Roorkee during 1983-1987. Currently she is working as an Associate Professor at Veermata Jijabai Technological Institute, Mumbai, India. Her research interests include Nano Electronics with emphasis on CNT, Compound semiconductors, High-k dielectrics and flash memories and Microwave communication.